

Application Number 09/737,540
Amendment dated October 7, 2003
Reply to Office Action of July 11, 2003

Amendments to the Claims

The listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

- B¹
1. (Currently Amended) A wiring of a semiconductor device comprising:
a first conductive layer formed on a semiconductor substrate;
a first insulation layer formed on said first conductive layer, planarized by a CMP process and having a scratch on a surface thereof;
a second insulation layer formed [[on]] immediately over said first insulation layer and contacting said first insulation layer;
a second conductive layer contacting said first conductive layer through a via hole formed in said first and second insulation layers; and
a third conductive layer formed in a groove formed in said second insulation layer, wherein said groove has a depth less than a thickness of said second insulation layer.
 2. (Original) A wiring of a semiconductor device as claimed in claim 1, wherein said first and second insulation layers are formed from a same insulation material.
 3. (Original) A wiring of a semiconductor device as claimed in claim 1, wherein said second conductive layer comprises a plug filling said via hole.
 4. (Original) A wiring of a semiconductor device as claimed in claim 1, wherein said first conductive layer is an impurity doped region on said semiconductor substrate.

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5. (Original) A wiring of a semiconductor device as claimed in claim 1, further comprising:

a third insulation layer formed on said second insulation layer, having a second via hole therein; and

B¹ a fourth conductive layer formed on said third insulation layer, contacting said third conductive layer through said second via hole.

6. (Original) A wiring of a semiconductor device as claimed in claim 5, wherein said fourth conductive layer is a bit line formed from a conductive material selected from a group consisting of tungsten, aluminum and copper.

7. (Currently Amended) A wiring of a semiconductor device comprising:
a first conductive layer formed on a semiconductor substrate;
a first insulation layer formed on said first conductive layer, planarized by a CMP process and having a scratch on a surface thereof;

a second insulation layer formed ~~[[on]]~~ immediately over said first insulation layer and contacting said first insulation layer and having a groove formed therein; and

a second conductive layer formed in said groove, the second conductive layer having a thickness thinner than a thickness of said second insulation layer.

8. (Original) A wiring of a semiconductor device as claimed in claim 7, wherein said first and second insulation layers are formed from a same insulation material.

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B1 9. (Original) A wiring of a semiconductor device as claimed in claim 7, wherein said second conductive layer is formed from a metal selected from a group consisting of tungsten, aluminum and copper.

Claims 10-17 Withdrawn
